Designing an Operational Amplifier

Angel Zhang
Electrical Engineering
The Cooper Union for the Advancement of Science and Art
Manhattan, NY

Jeffrey Shih
Electrical Engineering
The Cooper Union for the Advancement of Science and Art
Manhattan, NY

***Abstract*—This paper describes one approach to designing an operational amplifier. Two components necessary to this design are (1) a differential amplifier biased by a current source and (2) a Class AB push-pull output stage. Only discrete components can be used, notably resistors, capacitors, diodes and bipolar junction transistors (BJTs). A 12V power supply range must be used for the op-amp; the rails can be flexible as long as they contain this range. Biasing must be achieved with current sources; resistance bias networks cannot be used. Various op-amp specifications are measured and calculated.**

I. Introduction

An operational amplifier is a differential amplifier with a single ended-output that provides a very high voltage gain (ideally infinite, but typically 10^5 to 10^6 in practice). It also has a low output impedance to allow the output to swing across a large fraction of the power supply range. As it uses a differential amplifier in its design, it involves two inputs: noninverting and inverting. The output is positive when the noninverting input is more positive than the inverting input, and negative when the reverse occurs.

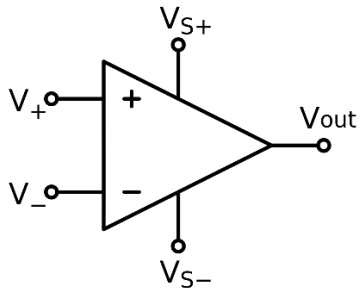

Fig. 1. Operational amplifier unit depicted as a black box

Op-amps are almost always used with feedback, in particular negative, where the output is coupled back into the input to partially negate it. Though the tradeoff is that this reduces the open voltage gain of the circuit to a high-loop-gain limit, feedback offers many desired characteristics such as mitigation of distortion, freedom from nonlinearity, flatness of frequency response, and predictability. Another bonus of using feedback is that the amplifier characteristics become more reliant on the feedback network rather than the open-loop amplifier, resulting in more control over the op-amp's properties.

There are two major characteristics ("golden rules") associated with an op-amp, and they are as follows:

1. The output, making using of negative feedback, attempts to make the voltage difference between the inputs zero. This is crucial, since even an infinitesimal voltage difference between the input terminals will result in a large output swing due to the absurd gain of the device.
2. The inputs, ideally, draw no current. In actual practice, they draw very little current.

II. Theoretical Design

As an op-amp incorporates a differential amplifier by definition, a differential amplifier is used an input stage for this design. This is also an appropriate choice due to the high input impedance of the differential amplifier as well as having a double ended input. A Class AB push-pull output stage is used to drive small loads effectively. In between these two stages, various amplification stages are implemented for both voltage and current gain.

A. The differential amplifier

In consideration of the properties of the op-amp as described in Section I, the differential amplifier must be designed (1) to have an appropriately high input impedance so the inputs draw as less current as possible and (2) to have a high voltage gain. To design for these criteria, small signal analysis can be used. Consider the simple example of a classic long-tailed pair, as shown in the figure below:

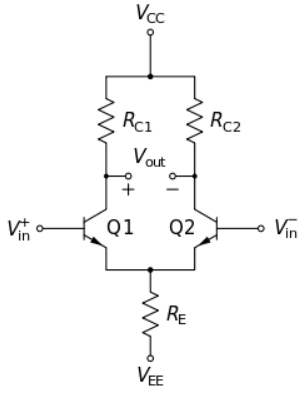

Fig. 2. Simple differential amplifier, classic long-tailed pair

Due to the symmetric nature of the circuit, small signal analysis can be conducted on one half circuit. Through simple inspection, one can deduce that this is a common emitter amplifier with emitter degeneration, for which the small signal voltage gain and input impedance can be expressed as:

$$|A_V| = \frac{\beta R_C}{r_\pi + 2(\beta + 1)R_E}$$

$$R_{in} = r_\pi + 2(\beta + 1)R_E$$

The pnp version of this differential amplifier, as shown in the figure below, will result in the same half circuit gain and input impedance.

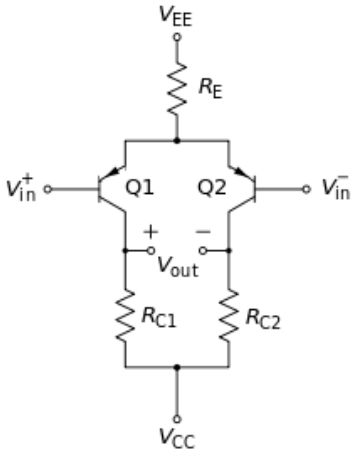

Fig. 3. Simple pnp differential amplifier

Using this model as the framework for our differential amplifier, it can be observed that making the collector resistances high relative to the emitter resistance will produce a high gain at the output. This can, of course, not only be achieved with resistors but components with appropriate impedances. Since a current source is used to the bias the differential amplifier at the joint-emitter junction of the npns, the impedance of the current source looking in from the emitter junction should be low relative to the impedance of whichever components are seen when looking in from the collectors. An active load is chosen for this purpose, more specifically, a current mirror, as depicted in Figure 4, and will provide a high impedance without resulting in a large DC voltage drop across it.

Though the input impedance of a common emitter with emitter degeneration is usually high due to the β amplification, the emitter resistance (in this case, the impedance of the current source) should be above a lower threshold.

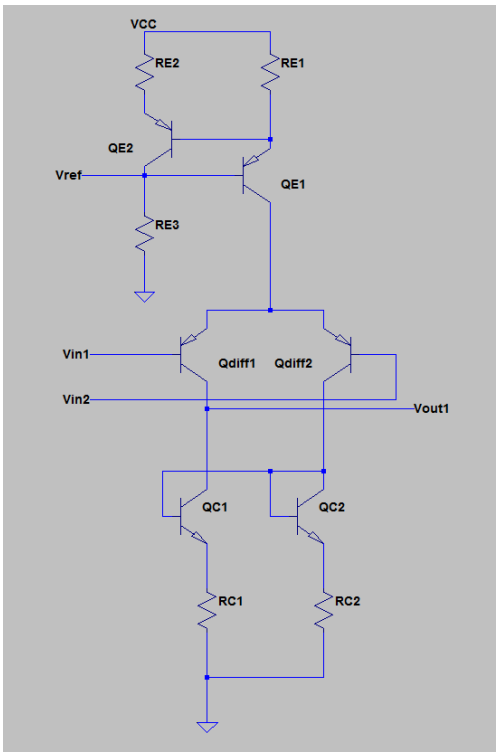

Fig. 4. Circuit diagram of differential amplifier in this op-amp

B. *The Class AB push-pull output stage*

The Class AB push-pull output stage is a variation on the Class B version that accounts for and eliminates crossover distortion. Typically, this is done by using diodes to maintain a voltage drop between the bases of output transistors and eliminate the deadband region. A drawback of this method is that it provides slight inaccuracies and distortion since a diode drop does not precisely match the transistors' base-emitter junction voltage V_{BE}. A better solution is to replace the diodes with diode-connected transistors that are matched to the output transistors. For this project, however, a third and even more elegant method is used to maintain the V_{BE} drop, namely using a V_{BE} multiplier.

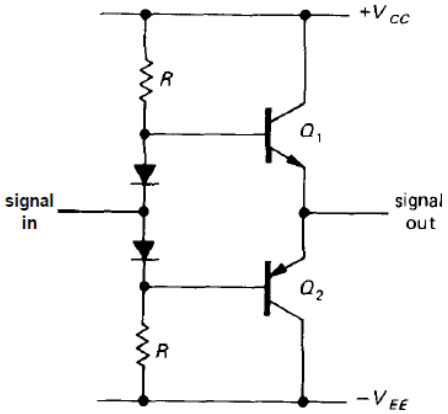

Fig. 5. Class AB push-pull output stage with diode biasing

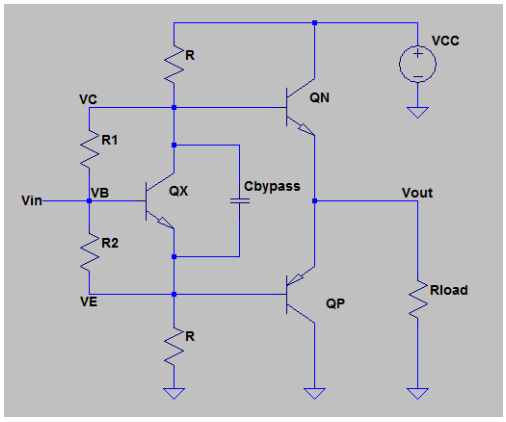

Fig. 6. Class AB push-pull output stage with a V_{BE} multiplier

The combination of Q_X, R_1, and R_2 makes up the multiplier, with the resistances acting as a stiff voltage divider network so that the current going through them is much greater than the current going through the bases of the output transistors Q_N and Q_P. Keeping this in mind, the collector-emitter voltage of Q_X can be found as follows:

$$V_{CE} = V_{CB} + V_{BE} = I_{BIAS}R_1 + V_{BE} = \frac{V_{BE}}{R_2}R_1 + V_{BE}$$

$$V_{CE} = \left(1 + \frac{R_1}{R_2}\right)V_{BE}$$

Hence, the drop across the two output transistor bases can be maintained as a multiple of V_{BE} depending on the values of $R_1$and R_2, and Q_X essentially acts like an adjustable diode. If the same transistor model as Q_N is used for Q_X, a near perfectly matching voltage drop can be achieved if the right resistors are used. In actual practice, two potentiometers can be used to tweak the resistances until crossover distortion is minimized, but for this lab, fixed resistors are used for simplicity. To maintain a stiff bias network, R_1 and R_2, should be no more than a few kΩ to draw more current from the power supply and also equal in order to maintain two V_{BE} drops across the two output transistor bases.

A capacitor C_{bypass} can be added in between the two output transistor bases to ensure that both transistors see the same signal, making the reproduction of the signal at the output more accurate. However, this may have a negative effect on the 3dB bandwidth and the gain bandwidth product of the op-amp, and is hence omitted for this project.

An alternative method of biasing the push-pull amplifiers, as opposed to using the resistors *R*, is to make use a current mirror as shown in Figure 7. This provides a much stiffer and more reliable biasing network. The input of the push-pull stage should also be biased by the previous stage so that there is enough room at each of the output transistor bases and the joint emitter for the desired peak-to-peak signal to swing (note: the headroom available is $V_{CC} - 2V_{BE} \approx 10.6\text{-}10.8V$).

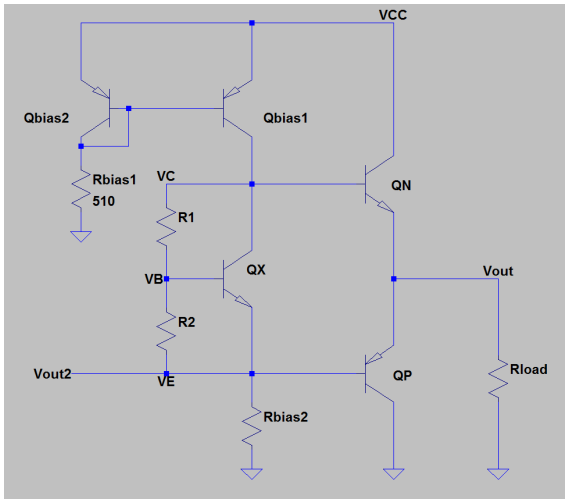

Fig. 7. Class AB push-pull output stage with current mirror biasing

C. *Intermediate amplification stages*

In order to provide additional voltage and current gain, a common emitter amplifier with emitter degeneration stage followed by a Darlington pair stage is incorporated in between the input and output stages. The output of the differential amplifier will directly bias the base of the common emitter, and the output of the Darlington pair will bias the input of the push-pull amplifier. The voltage gain is given by:

$$|A_V| = \frac{\beta\left(R_{C,amp1} \parallel R_{load}\right)}{r_{\pi,Q_{amp1}} + \left(\beta_{Q_{amp1}} + 1\right)R_{E,amp1}}$$

where R_{load} represents the input impedance of the Darlington pair, yet it should not decrease the gain that much since the Darlington stage acts as an impedance transformer with high input impedance and low output impedance. The current gain will just be $\beta_{amp2}\beta_{amp3} = \beta_{amp}^2$, since the two Darlington transistors are matched.

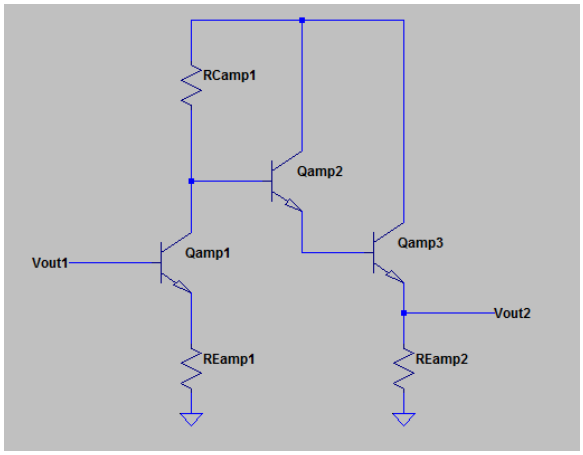

Fig. 8. Intermediate amplification stages consisting of a current emitter with degeneration followed by a Darlington pair

D. The complete op-amp

The operational amplifier design in its entirety, including all transistor models and resistor values, is depicted in the figure below:

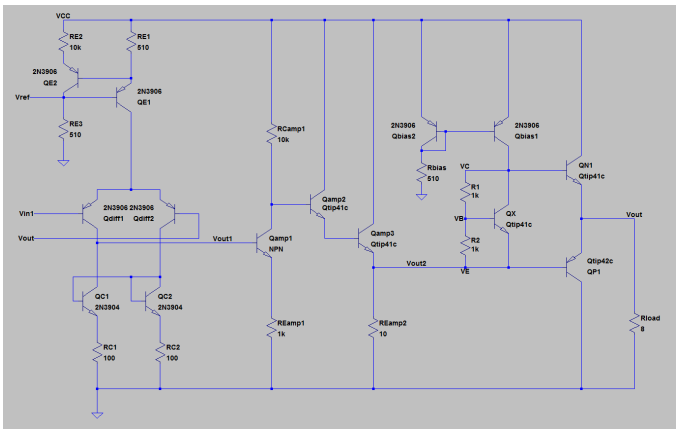

Fig. 9. Complete op-amp with actual models and values

The effects of the chosen resistor values will be explained in the subsequent sections, where they manifest themselves in various op-amp specs. The TIP41C and TIP42C transistors are used when sourcing higher currents (heat sinks are used with these transistors when building the actual circuit).

III. Specifications

When designing an op-amp, it is important to consider its specs and their standards for use in a larger scale system such as an embedded system. The following specs are quantified for this particular op-amp: (1) the open-loop gain, (2) the gain-bandwidth product, (3) the common-mode input voltage range, (4) the input offset voltage, (5) the common-mode rejection ratio (CMRR), and (6) the power-supply rejection ratio (PSRR).

(1) The open-loop gain is the voltage gain of the op-amp while not in feedback mode. Ideally, this is infinity, but that is not practical in real application.

(2) The gain-bandwidth product is the product of the op-amp's bandwidth and the gain at which the bandwidth is measured. This can be easily measured when the op-amp is in unity-gain mode, where the output terminal is fed back into the inverting input terminal. Here, the gain-bandwidth product is just the bandwidth of the circuit.

(3) The common-mode input voltage range is the range of common-mode input voltages that results in proper operation.

(4) The input offset voltage is the largest differential DC voltage between the two inputs of the op-amp required to make the output zero. A special test circuit, shown in the following figure, can be used to find this voltage. The offset voltage V_{IO} can then be found by dividing by 1001 the output voltage of the op-amp in this configuration when there is no common-mode input (both input terminals are grounded).

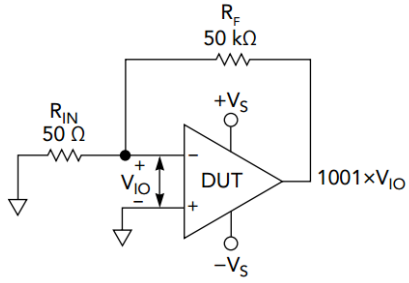

Fig. 10. Test circuit to find the input offset voltage

(5) The common-mode rejection ratio of an op-amp measures its ability to reject common-mode signals. It can be calculated by using the formula:

$$\mathrm{CMRR} = \left|\frac{\mathrm{A_d}}{\mathrm{A_{cm}}}\right|$$

$$\mathrm{CMRR(dB)} = 20\log_{10}\left|\frac{\mathrm{A_d}}{\mathrm{A_{cm}}}\right|$$

where $\mathrm{A_d}$ is the differential mode gain of the op-amp and $\mathrm{A_{cm}}$ is the common-mode gain. Alternatively, the CMRR can be found using the circuit configuration in Figure 10 by applying a common-mode voltage to the op-amp's noninverting input. The CMRR can then be calculated using:

$$\mathrm{CMRR} = \left|\frac{\Delta \mathrm{V_{in,(+)}}}{\Delta \mathrm{V_{IO}}}\right|$$

$$\mathrm{CMRR(dB)} = 20\log_{10}\left|\frac{\Delta \mathrm{V_{in,(+)}}}{\Delta \mathrm{V_{IO}}}\right|$$

(6) Lastly, the power-supply rejection ratio of an op-amp describes its ability to reject noise from its power supply. It can be calculated by using the formula:

$$\mathrm{PSRR} = \left|\frac{\mathrm{A_v}}{\mathrm{A_{supply}}}\right|$$

$$\mathrm{PSRR(dB)} = 20\log_{10}\left|\frac{\mathrm{A_v}}{\mathrm{A_{supply}}}\right|$$

where $\mathrm{A_v}$ is the open-loop gain of the op-amp and $\mathrm{A_{supply}}$ is the power supply gain. Alternatively, the PSRR can be found using the circuit configuration in Figure 10 by changing the supply voltage of the op-amp. The CMRR can then be calculated using:

$$\mathrm{PSRR} = \left|\frac{\Delta \mathrm{V_{supply}}}{\Delta \mathrm{V_{IO}}}\right|$$

$$\mathrm{PSRR(dB)} = 20\log_{10}\left|\frac{\Delta \mathrm{V_{supply}}}{\Delta \mathrm{V_{IO}}}\right|$$

IV. Simulation Results

SIMULATIONS of the complete op-amp shown in Figure 9 are made in LTSpice in order to measure the specs detailed in Section III.

A. Open-loop gain

The open loop gain can be observed by measuring either the circuit's output voltage swing or its frequency response for given inverting and noninverting inputs. However, both are important to test for the sake of ensuring proper circuit operation, since the output voltage swing allows for the detection of clipping and distortion at different voltages, and the frequency response allows for the detection of distortion at different frequencies.

The output voltage is measured by conducting a transient analysis with two 1kHz, 0.1mV peak-to-peak input sine waves with a common-mode of 6V that are completely out of phase with one another. Thus, the differential input is a 0.2mV peak-to-peak centered about a 6V DC offset. The output swing is measured to be 3.53V peak-to-peak centered about a DC offset of 5.59V, which corresponds to a gain of ~17,650, or 85dB.

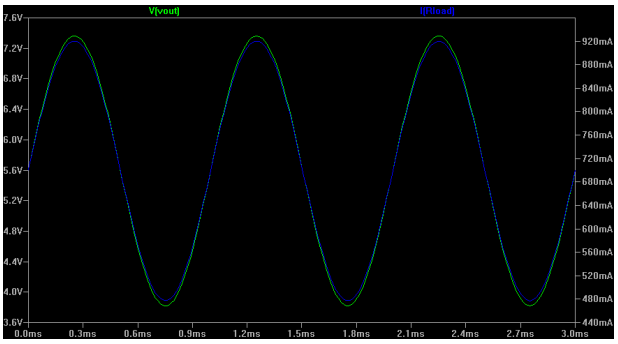

Fig. 11. Output swing of op-amp using a 0.2mV peak-to-peak differential input centered about a 6V DC offset

The frequency response is measured by conducting an AC analysis with the same input sine waves used in the transient analysis. The gain is ~85dB in the op-amp's operating region (which is consistent with the previous analysis), and the 3dB bandwidth is ~250k-270kHz.

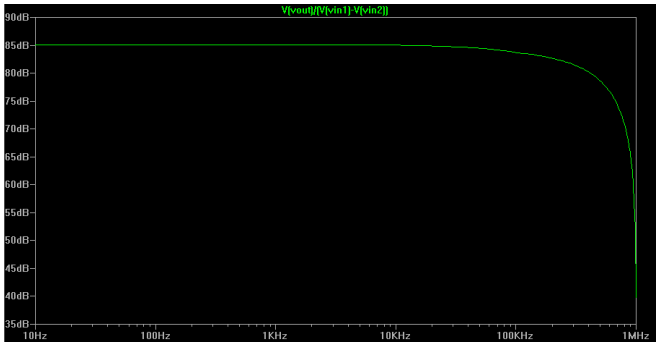

Fig. 12. Frequency response of op-amp

B. Gain-bandwidth product

Before finding the gain-bandwidth product, the output voltage of the circuit is simulated in unity-gain mode. The input to the noninverting input is a 1kHz, 1V peak-to-peak sine wave with a DC offset of 5V. For unknown reasons, there is a ridiculously high run time when the exact model of intermediate stage transistors are specified (perhaps because of a constant need to fill in the transistor type due to the iterative nature of the feedback circuit), so they were left as the default model NPN. This issue will be explored at a future date.

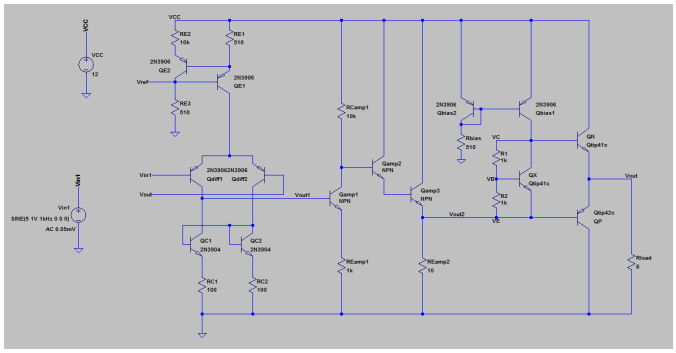

Fig. 13. The op-amp in unity gain mode ($v_{in2} = v_{out}$)

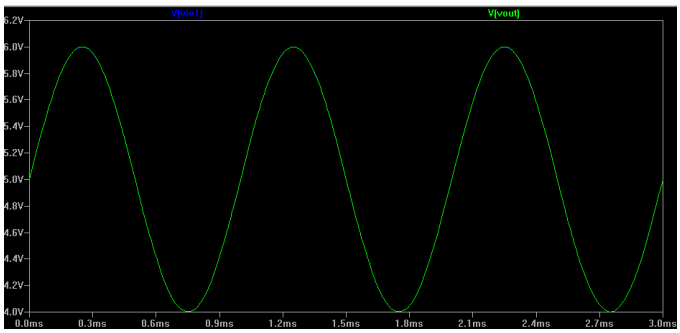

Fig. 14. Output swing of op-amp in unity gain mode compared to the input swing

The gain-bandwidth product is then found from the frequency response of the circuit in unity-gain mode. It is shown that the gain remains consistent at ~931-933μdB until it starts to grow exponentially at around 200kHz. However, since the initial rate of growth of the curve is low, the frequency response will remain relatively flat at a finite range of frequencies above 200kHz. As an approximation, the gain bandwidth product is taken to be the frequency where the gain starts to deviate from unity by just over 1mdB, which is around 505-518kHz.

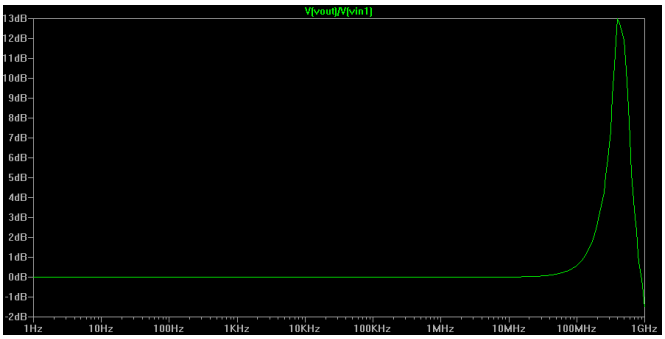

Fig. 15. Frequency response of op-amp in unity-gain mode

C. Common-mode input voltage range

The common-mode input range is found to be about 3.9V to 6V through a series of transient analyses on circuits with different common modes. Beyond these two points, the op-amp cannot function properly, as the output experiences clipping or distortion.

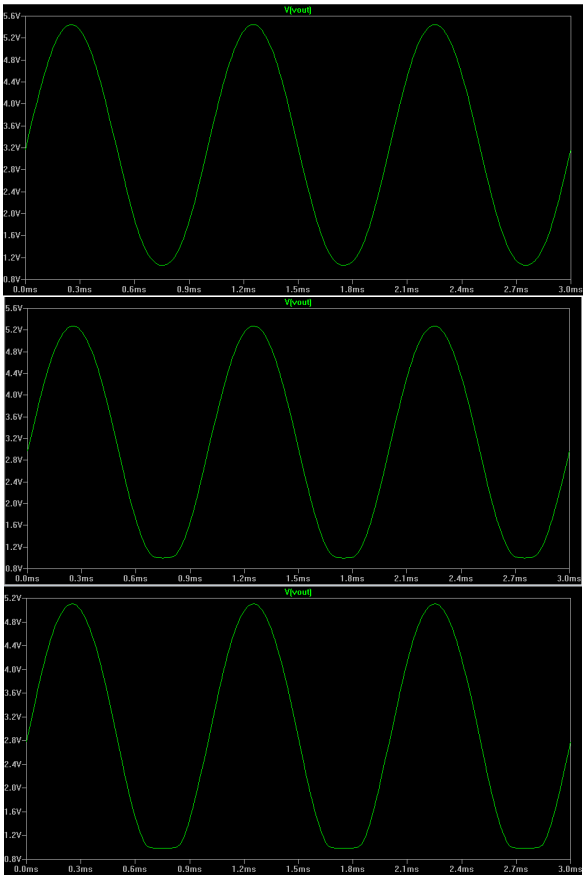

Fig. 16. Lower bound of common-mode input voltage range. At 3.9V (top), the output experiences no distortion. At 3.8V (middle), the output experiences slight clipping at its negative cycle. At 3.7V (bottom), clipping is more profound.

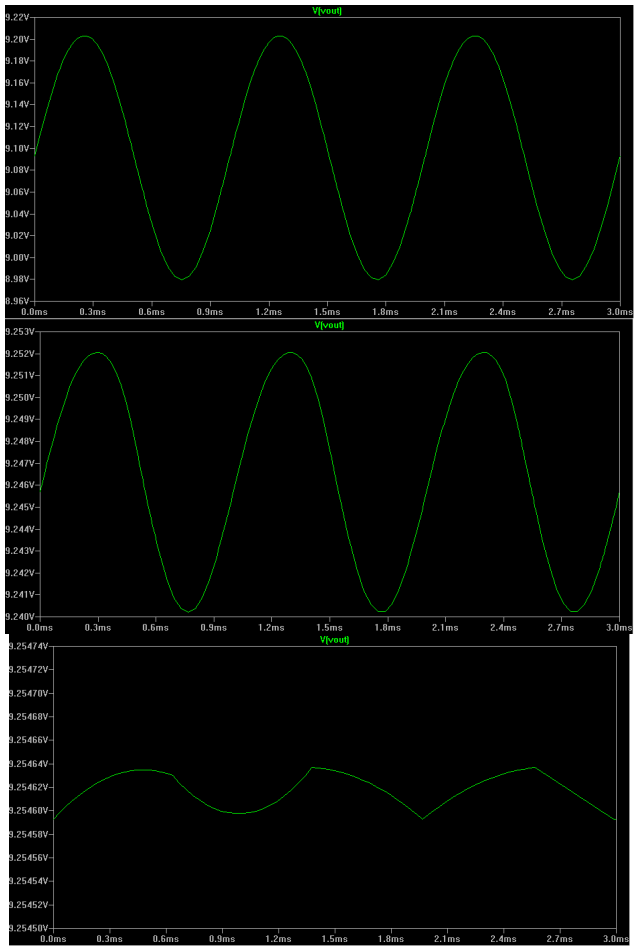

Fig. 17. Upper bound of common-mode input voltage range. At 6V (top), the output experiences no distortion. At 6.1V (middle), the output experiences slight distortion. At 6.2V (bottom), distortion is significant.

D. *Input offset voltage*

Using the test circuit described in Figure 10, the input offset voltage is found by running a DC operating point analysis for the simulation circuit in Figure 18 to find its output voltage, resulting in:

```
V(vout):        7.4295          voltage
```

The input offset voltage is then calculated to be $V_{IO} = \frac{V_{out}}{1001} = \frac{7.4295V}{1001} = 7.422mV$.

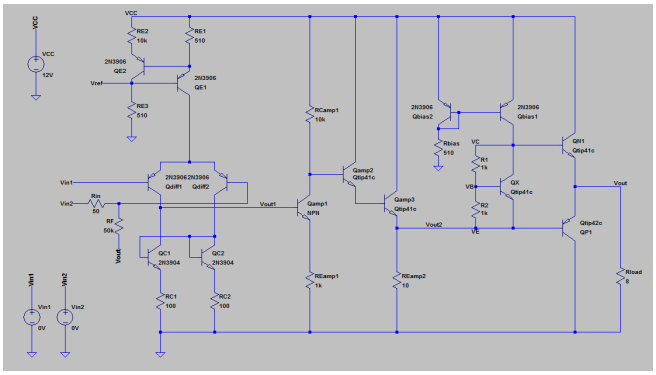

Fig. 18. Simulation circuit used to calculate offset voltage

E. *Common-mode rejection ratio*

Since the input offset voltage for when the common-mode input voltage is 0V has been found in Section IV.C, only an input offset voltage for another common-mode voltage is needed to find the CMRR. A DC operating point analysis is conducted after V_{in1} is increased to 5V, yielding:

```
V(vout):        9.25429         voltage
```

The CMRR is then found by:

$$\text{CMRR} = \left| \frac{5V - 0V}{\frac{1}{1001}(9.25429V - 7.4295V)} \right| = 2742.78$$

$$\text{CMRR(dB)} = 20\log_{10}|2742.78| = 68.76\text{dB}$$

F. *Power-supply rejection ratio*

Since the input offset voltage for when the common-mode supply voltage is 12V has been found in Section IV.C, only an input offset voltage for another supply voltage is needed to find the PSRR. A DC operating point analysis is conducted after V_{CC} is decreased to 6V, yielding:

```
V(vout):        3.43737         voltage
```

The PSRR is then found by:

$$\text{PSRR} = \left| \frac{6V - 12V}{\frac{1}{1001}(7.4295V - 3.43747V)} \right| = 1504.5$$

$$\text{CMRR(dB)} = 20\log_{10}|1504.5| = 63.55\text{dB}$$

V. Empirical Results

To experimentally test the op-amp design, the circuit is built on a perfboard. Inputs are generated using function generators with the capability to produce a DC offset, and results were observed on an oscilloscope.

Note to professor: Due to time constraints, the PSRR is not measured. Some more oscilloscope diagrams could have also been added. Sorry!

A. *Open-loop gain*

To find the open loop gain, the output is measured by applying only a 0.2mV, 1kHz, peak-to-peak sine wave to the noninverting input centered about a DC offset of 6V. Since the function generator is only able to produce signals as low as 20mV peak-to-peak, a voltage divider is used to attenuate the generated wave. The voltage gain is measured to be ~83dB.

B. *Gain-bandwidth product*

The op-amp is first successfully tested in unity gain mode by applying an input of 2V peak-to-peak as shown in Figure 19, then the gain bandwidth product is found by consistently increasing the voltage. The output begins to exhibit a ringing effect past 480kHz due to the high slew rate, so the gain bandwidth product is taken to be 480kHz.

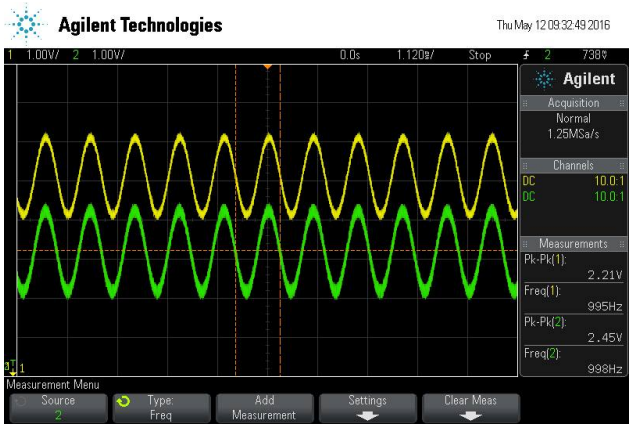

Fig. 19. Op-amp output in unity gain mode.

Note to professor: The noise is due to an issue with the breadboard that was used. Using another spot on the breadboard yielded a noiseless output wave, but we forgot to capture this.

C. Common-mode input voltage range

The common-mode input range is found by applying a function generator with a DC offset to the noninverting input while applying the same DC voltage to the inverting input using a power supply. The DC offset and power supply are changed simultaneously across a wide range of voltages. The operating range of the circuit is found to be 4-6V.

D. Input offset voltage

The input offset voltage is measured by using the test circuit in Figure 10. Corresponding to no common-mode input, $V_{out} = 0.08V$, so $V_{IO} \approx 0.08mV$.

E. Common-mode rejection ratio

Using the output voltage found in Section V.D and the measured output voltage corresponding to a common-mode of 6V ($V_{out} = 0.38V$), the CMRR is calculated to be:

$$\text{CMRR} = \left| \frac{6V - 0V}{\frac{1}{1001}(0.38 - 0.08V)} \right| = 20020$$

$$\text{CMRR(dB)} = 20\log_{10}|20020| = 86.03\text{dB}$$

F. Power-supply rejection ratio

This is not measured due to time constraints.

G. Data Tables

Specifications

Spec	Simulation	Empirical
Open-loop gain	~85dB	~83dB
Gain-bandwidth product	505-520kHz	480kHz
Common-mode input voltage range	3.9-6V	4-6V
Input offset voltage	7.422mV	0.08V
CMRR	68.76dB	86.03dB
PSRR	63.55dB	N/A

Summarizing these results, the empirical open-loop gain, gain-bandwidth product, and common-mode input voltage range match closely with the simulated results and meet the expectations that they are slightly worse than predicted. However, the input offset voltage and CMRR are inexplicably different; in particular, the CMRR is almost 20dB higher, much better than predicted. Overall, the op-amp specifications are very acceptable, since there is a high open-loop gain, a large gain-bandwidth product, a low input offset voltage, and a high CMRR.

VI. Conclusion

As in many real-world applications of circuits, it is difficult to design to meet ideal specifications, but designs can nevertheless be optimized to approach ideal operation. Using discrete components to design an operational amplifier, as is done for this report, is also advantageous to using analog op-amps due to more flexibility in controlling the device's specs. For this lab, the main focus is to produce a massive gain befitting the definition of an op-amp; the other specs are just measured and tested as a quality check. Future endeavors can be made to manipulate these specs and specialize the device for use in certain applications.