

Designing an Audio Amplifier Using a Class B Push-Pull Output Stage

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Abstract—This paper describes one approach to designing an audio amplifier using a Class B push-pull output stage in conjunction with other discrete circuit components, notably resistors, capacitors, diodes and bipolar junction transistors (BJTs). Requirements are that (1) 10-12V peak-to-peak output must be produced from a 0.2mV peak-to-peak input that is first amplified by a common emitter stage to produce a 1V peak-to-peak signal and (2) the high and low 3dB points are <100Hz and >22kHz, respectively. Two voltage supplies can be used: a 5V supply to power the common emitter stage, and a 12V supply for the rest of the circuit including the push-pull stage.

I. INTRODUCTION

THE Class B push-pull output stage is a power amplifier that uses two active devices to deliver power, with each device conducting for alternate half cycles. Typically, this is realized by using both an npn and pnp BJT transistor in the configuration shown in the following figure.

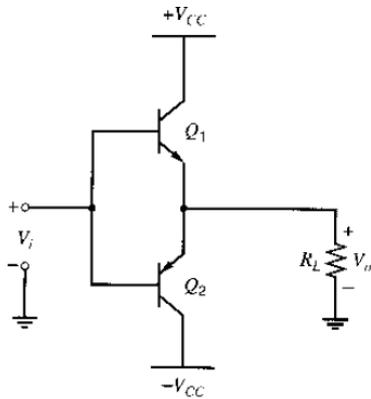


Fig. 1. Simple Class B push-pull output stage

The major drawback of the class B push-pull output stage is crossover distortion, which results a deadband of $2V_{BE}$ centered around $v_{in} = 0$ when plotting v_{in} against v_{out} . This arises because when $|v_{in}| < V_{BE}$ for either transistor, both transistors are off and the output will remain at 0V. When $v_{in} > V_{BE1}$, Q1 is on and Q2 is off and the output will follow the input since Q1 is an emitter follower. This generates the positive half cycle of the output. A similar phenomenon occurs when $v_{in} < -V_{BE2}$, except the negative half cycle of the output is produced.

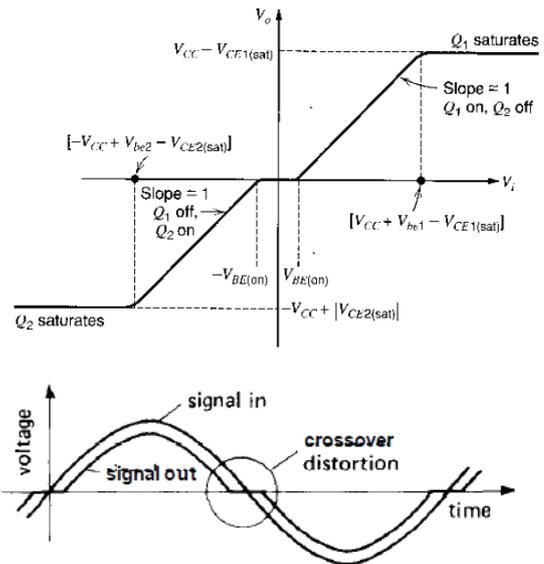


Fig. 2. Transfer characteristic and signal vs. time plot of Class B push-pull output stage, illustrating crossover distortion

Effects of crossover distortion are mitigated for larger input signals, but eventually the output signal will clip for large enough signals since Q1 and Q2 head into saturation. A common remedy for crossover distortion is the use of the Class AB variation of the push-pull output stage.

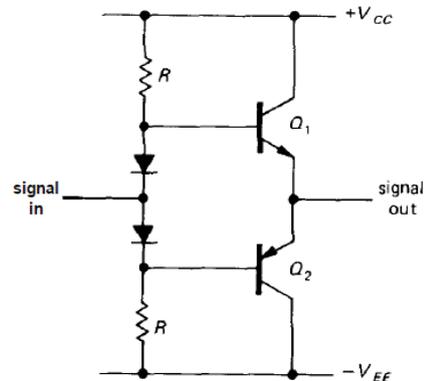


Fig. 3. Class AB push-pull output stage

The bias resistors, denoted by R , force current conduction through the diodes and hence maintains a cumulative voltage drop of 1.4V (0.7V for each diode) from the base of Q1 to the base of Q2. Now, even when $|v_{in}| < V_{BE}$, the base-emitter junctions of transistors are biased such that one transistor is always on and the full input signal is carried over to the output with the deadband minimized.

Another issue of the Class B amplifier is that it is thermally unstable. A phenomenon called thermal runaway occurs when the temperature of the transistors rises and causes a drop in V_{BE} , which in turn leads to a greater flow in quiescent collector current I_C . To prevent I_C from becoming too high, resistors can be incorporated into the emitters of the transistors. This introduces negative feedback and causes V_{BE} to rise whenever I_C rises, hence stabilizing the circuit.

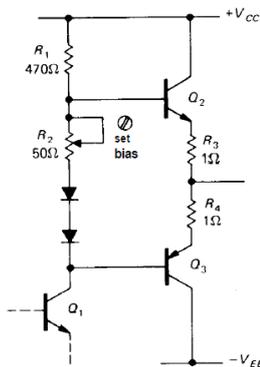


Fig. 4. Class AB push-pull output stage, addressing the effects of thermal runaway

II. THEORETICAL DESIGN

IN order to produce a 10-12V peak-to-peak output swing with a 0.2mV peak-to-peak input, the amplifier must achieve an aggregate voltage gain of 500-600, or 54-56dB. Since the voltage gain of a push-pull amplifier is approximately unity because it is composed of emitter followers, there must be at least one voltage amplifying stage before it. It is required to use a common emitter amplifier that achieves a gain of 50 (34dB) to output a 1V peak-to-peak signal given the 0.2mV peak-to-peak input, so another amplification stage must be included to provide an additional gain of 10-12 (20-22dB).

A. The first common emitter stage

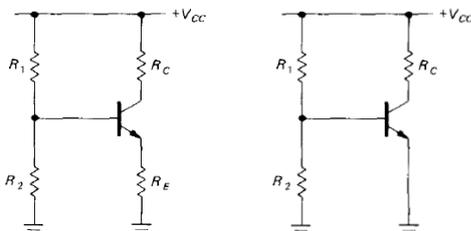


Fig. 5. Common emitter amplifier with (left) and without (right) degeneration

When designing a common emitter amplifier, there are generally two options to go about: with or without emitter degeneration. The former produces a well-defined gain $|A_v| = \frac{\beta R_C}{r_{\pi} + (\beta + 1)R_E}$, while the latter produces a higher but β -dependent gain $|A_v| = g_m R_C = \frac{I_C}{V_T} R_C$, where I_C is the quiescent collector current and V_T is the thermal voltage. Since a high but β -independent gain is desired for this stage, the common emitter with degeneration is selected as a starting point to be imbued with slight modifications. The following diagram depicts the design of choice.

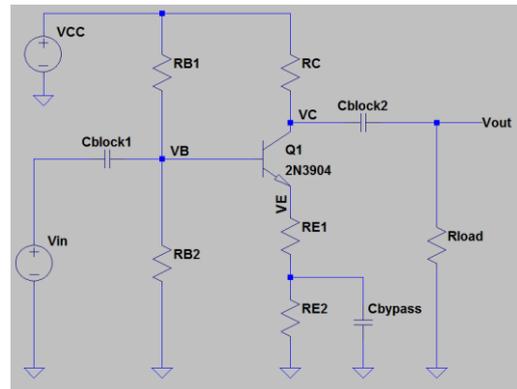


Fig. 6. Common emitter amplifier design with two emitter resistors, one bypassed using a capacitor

In small signal operation, the circuit behaves like an emitter degenerated amplifier because only a fraction of the total emitter resistance $R_E = R_{E1} + R_{E2}$ is bypassed by the capacitor C_{bypass} ; R_{E1} will still help define the gain. However, R_{E2} is chosen to be much larger than R_{E1} such that in large signal operation, it will dominate the total emitter resistance and hence be the major factor in determining the quiescent collector current. This disassociates the task of designing for gain from biasing the quiescent points (albeit, not completely), and provides more flexibility in the design of the amplifier.

First and foremost, the quiescent emitter and collector node voltages V_E and V_C , respectively, must be biased such that the input and output signals have enough room to swing for a given V_{CC} , which is 5V in this case. V_E must be biased to at least the amplitude of the input signal. Here, the input is only 20mV peak-to-peak, so V_E can be biased to a low value. To ensure that the output swing does not conflict with the input swing, V_C should be biased to at least $V_E + v_{in,max} + V_{BE} + v_{out,max}$, where $v_{in,max} = 10mV$ and $v_{out,max} = 0.5V$ represent the amplitudes of the input and output signals, respectively, and the base-emitter junction voltage V_{BE} is 0.65V at the minimum for $I_C = 1mA$ (according to the 2N3904/2N3906 transistor datasheet). This is a result of the condition that the collector node voltage must be greater than the base node voltage, i.e. $v_C > v_B$, in the forward active operating region of the BJT. Finally, $V_C + v_{out,max}$ must not exceed V_{CC} , or the positive half cycle of the output will clip. The above conditions can be summarized as follows:

- i. $v_{in,max} < V_E < V_C - (v_{out,max} + V_{BE} + v_{in,max})$
 $10mV < V_E < V_C - 1.16V$
- ii. $V_E + v_{in,max} + V_{BE} + v_{out,max} < V_C < V_{CC} - v_{out,max}$
 $V_E + 1.16V < V_C < 4.5V$

Next, an appropriate collector current must be selected. Since $I_C \approx I_E$, where I_E is the quiescent emitter current, the following equality holds:

$$I_C = \frac{V_{CC} - V_C}{R_C} \approx \frac{V_E}{R_E} = I_E$$

Hence, selecting the quiescent collector current will allow the determination of R_C and subsequently R_E since the gain is known and relates R_C and R_E .

Now, I_C can be selected, but this must be done while keeping in mind a certain tradeoff. To achieve a high gain, a larger R_C relative to R_{E1} is desired, so one might want to choose a smaller I_C . However, doing so not only increases the value of R_C but r_π as well, since $r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C}$ and is inversely related to I_C . If r_π becomes too large, it will not be dominated by $(\beta + 1)R_E$ in the denominator of the gain expression and the gain will be more β -dependent.

Using $I_C = 1.6mA$, $R_C = 1k\Omega$, $R_{E1} = 1\Omega$, and $R_{E2} = 820\Omega$ puts V_C at $\sim 3.4V$ and V_E at $\sim 1.3V$. Furthermore, by taking into account a range of β values from 50 to 300 and $V_T = 25mV$ at room temperature, a β -independent gain ranging from 59 to 60 is calculated for when the circuit drives an infinite impedance load. This results in a 1.2V peak-to-peak output, resulting in a low of 2.8V and a high of 4V for the collector voltage v_C , but this is fine since the threshold voltages of $V_E + V_{BE} + v_{in,max} \approx 2V$ and $V_{CC} = 5V$ are not crossed. In addition, the actual load will have a finite impedance, bringing the gain down. When driving a 5k Ω load, the amplifier is calculated to have a gain of 49-50, which still meets the requirement.

To keep the quiescent points in place, a stiff voltage divider is used as a bias network in conjunction with a DC-blocking capacitor C_{block} at the base. Since $V_E \approx 1.3V$, the quiescent base node voltage $V_B = V_E + V_{BE} = V_E + 0.65V \approx 2V$. In addition, the quiescent base current I_B should be negligible compared to the current flowing through the bias network I_{BIAS} (at most a tenth of the amount). This can be expressed as follows:

$$\begin{aligned} I_{BIAS} &\gg I_B \\ \frac{V_{CC}}{R_{B1} + R_{B2}} &\gg \frac{I_C}{\beta} \\ R_{B1} + R_{B2} &< \frac{\beta V_{CC}}{10I_C} \end{aligned}$$

According to the 2N3904/2N3906 data sheet, $\beta = 80$ for $I_C = 1mA$, so the approximation that $\beta \approx 100$ is used to find the maximum cumulative base resistance, which is around 30k Ω . To bias the base at 2V, the values $R_{B1} = 10k\Omega$ and $R_{B2} = 15k\Omega$ can be used, the sum of which is under 30k Ω .

To ensure that this stage is able to drive the next one without depreciating the gain significantly, the output is connected to the base of an emitter follower to be used as an impedance transformer. The emitter resistance of the follower is arbitrarily chosen to be 1k Ω , though it should not too big or there is not enough current to drive the load. It should also not be too small, or the output will not have enough room to swing on its negative cycle. Simulations have shown that this setup can drive as low as a 1k Ω load while maintaining a 1V peak-to-peak output swing (see Section III).

Time-constant analysis is used ensure that the bandwidth specifications are met at this stage. The lower frequency bound can be found using infinite value time constants through the following equations:

$$\begin{aligned} \omega_L &= \frac{1}{2\pi \sum \tau} = \frac{1}{2\pi(\tau_B + \tau_C + \tau_E)} \\ \tau_B &= R_{block1}^\infty C_{block1} = [R_{B1} \parallel R_{B2} \parallel (r_\pi + (\beta + 1)R_{E1})]C_{block1} \\ \tau_C &= R_{block2}^\infty C_{block2} = (R_C \parallel R_{load})C_{block2} \\ \tau_E &= R_{bypass}^\infty C_{bypass} \approx R_{E1}C_{bypass} \end{aligned}$$

However, results from the theoretical analysis are found to be very distinct from simulation results, so capacitances are selected during simulation instead. Standard capacitances of 33 μF are chosen for the blocking capacitors, but it is found that picking a larger emitter bypass capacitor, specifically 470 μF , produces a better result for the lower 3dB point. A similar analysis can be done to find the higher 3dB point using zero value time constants, but this is not necessary since the simulated upper bound extends far beyond the desired upper bound of 22kHz.

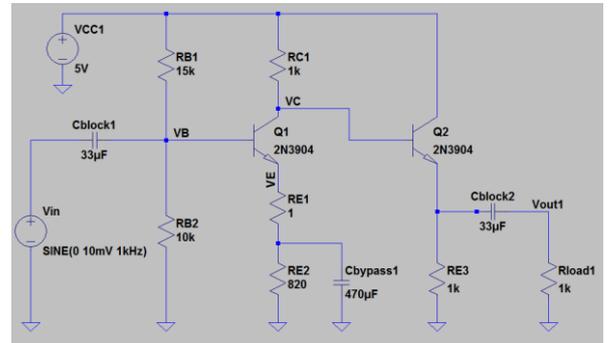


Fig. 7. Overall first stage, common emitter followed by an emitter follower

B. The second common-emitter stage

Designing the second common emitter stage is similar to designing the first, except that there is much less headroom available relative to the amplitude of the desired output signal, leading to tighter constraints on circuit design. 12V are available from the power supply; after subtracting 1V for the input swing and an additional 0.65V-0.85V for V_{BE} (the range listed in the 2N3904/2N3906 datasheet), only around 10.15V-10.35V are available for the output. Thus, quiescent point biasing needs to be more precise, since there is less than a 0.5V margin of error for centering the output signal.

Since the gain for the second stage is much less than the gain of the previous stage, a higher quiescent collector current can be afforded. This is favorable, since a high current is desired in order to better drive the output stage. As a result, the emitter and collector resistances need to be low; this makes it inconvenient to split the emitter resistance into further smaller values as in the previous stage, so a simple emitter degenerated amplifier without a bypass capacitor is utilized for this stage (refer to Fig. 5, left).

Selecting $I_C = 10\text{mA}$, $R_C = 520\Omega$, and $R_E = 50\Omega$ puts V_C at $\sim 6.7\text{V}$ and V_E at $\sim 0.5\text{V}$. The maximum and minimum values of v_C are hence 1.7V and 11.7V . Using $V_{BE} \approx 0.7\text{V}$ corresponding to the value of I_C , the upper threshold of $V_{CC} = 12\text{V}$ and the lower threshold of $V_E + V_{BE} + v_{in,max} = 1.7\text{V}$ are not violated, though barely. Due to fluctuations in V_{BE} , there may be slight clipping for the negative half cycle, but it should not have a significant effect on the output. Calculating the gain using a range of β values from 60 to 300 results in values ranging from 9.7 to 9.9 for an infinite load. The collector resistor can be slightly increased to improve the gain at the cost of slight clipping of the output signal. It will be shown via simulation (see Section III) that a value of 550Ω for R_C is actually preferred.

Once again using a bias network and following the same rules for biasing the quiescent points, the maximum cumulative base resistance is found to be $12\text{k}\Omega$. To bias the base at $V_E + V_{BE} = 1.2\text{V}$, the values $R_{B1} = 10.8\text{k}\Omega$ and $R_{B2} = 1.2\text{k}\Omega$ can be used, the sum of which is exactly $12\text{k}\Omega$.

To ensure that enough current is available to drive the push-pull output stage, a Darlington pair is used as an impedance transformer and is connected in series with the output of the circuit. The emitter resistance of the Darlington should be extremely low to draw more current. The value for this resistance is chosen empirically through simulation, and the optimal value is found to be 20Ω . The overall stage has been shown in simulation to be able to drive load impedances as small as 200Ω without changing the output signal.

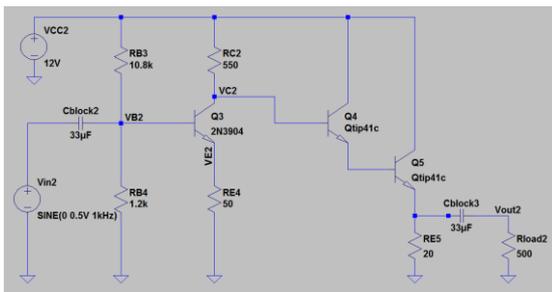


Fig. 8. Overall second stage, common emitter followed by a Darlington pair

C. The push-pull output stage

The Class AB push-pull circuit, as discussed in Section III, is the amplifier of choice for this audio amplifier, though with a variation on its biasing. Using diodes to maintain a voltage drop between the bases of the npn and pnp transistors will provide inaccuracies and slight distortion since a diode drop does not precisely match the transistors' base-emitter junction voltage V_{BE} . An alternative and more precise method for maintaining this drop is to use a V_{BE} multiplier, illustrated in the figure below.

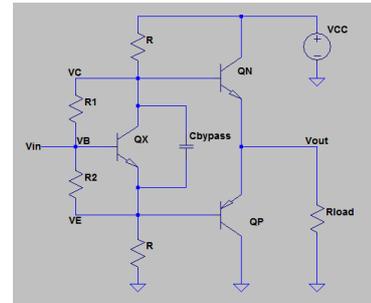


Fig. 9. A V_{BE} multiplier, as used in a push-pull output stage

The combination of Q_X , R_1 , and R_2 makes up the multiplier, with the resistances acting as a stiff voltage divider network so that the current going through them is much greater than the current going through the bases of the output transistors Q_N and Q_P . Keeping this in mind, the collector-emitter voltage of Q_X can be found as follows:

$$V_{CE} = V_{CB} + V_{BE} = I_{BIAS}R_1 + V_{BE} = \frac{V_{BE}}{R_2}R_1 + V_{BE}$$

$$V_{CE} = \left(1 + \frac{R_1}{R_2}\right)V_{BE}$$

Hence, the drop across the two output transistor bases can be maintained as a multiple of V_{BE} depending on the values of R_1 and R_2 , and Q_X essentially acts like an adjustable diode. If the same transistor model as Q_N is used for Q_X , a near perfectly matching voltage drop can be achieved if the right resistors are used. In actual practice, two potentiometers can be used to tweak the resistances until crossover distortion is minimized, but for this lab, arbitrary resistors are selected for simplicity. A capacitor C_{bypass} is added in between the two output transistor bases to ensure that both transistors see the same signal, making the reproduction of the signal at the output more accurate.

To maintain a stiff bias network, resistances should be no more than a few $\text{k}\Omega$ to draw more current from the power supply. The V_{BE} multiplier resistors, R_1 and R_2 , are selected to be $1\text{k}\Omega$ to maintain two V_{BE} drops across the two output transistor bases. The pull-up and pull-down resistors, denoted by R in Fig. 8, are also arbitrarily selected to be $330\text{k}\Omega$. Thermal runaway is not accounted for in the design of this circuit since adding the emitter resistors will lead to a slight gain drop, though they should be included in standard practice.

The push-pull stage should also be biased properly so that there is enough room at each of the output transistor bases and the joint emitter for the 10V peak-to-peak signal to swing (note: the headroom available is $V_{CC} - 2V_{BE} \approx 10.6-10.8V$). The previous stage can be used to achieve this task: recall that the quiescent collector node voltage of the second common emitter is biased at $\sim 6.7V$, meaning that the quiescent emitter node voltage of the Darlington pair is $2V_{BE}$ less, or $\sim 5.2V$ ($V_{BE} \approx 0.7-0.8V$ for $I_C = 0.1-1A$ according to the TIP41C/TIP42C datasheet). If the output of the Darlington is directly connected to the base of the pnp transistor in the push-pull stage, the base of the npn will be biased at $\sim 6.7V$, and thus the output will be biased at $\sim 6V$. Thus, the signal has enough room to swing at each of these terminals and there will be minimal clipping.

The overall circuit is depicted in the diagram below, and its operation is simulated in LTSpice (discussed in Section III).

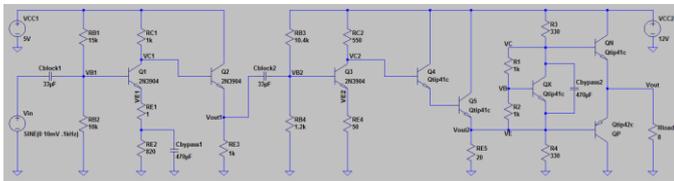


Fig. 10. Complete audio amplifier circuit

III. SIMULATION RESULTS

BEFORE simulating the entire circuit, the stages are simulated one at a time to ensure that they are working individually. The following figures include both the DC operating point values and time versus v_{out} graphs obtained from conducting a DC and transient analysis at the output of each stage, respectively.

A. The first common emitter stage

--- Operating Point ---

V(vb):	1.96872	voltage
V(vc):	3.41064	voltage
V(ve):	1.30177	voltage
Ic(Q1):	0.00158037	device_current
Ib(Q1):	5.21326e-006	device_current
Ie(Q1):	-0.00158559	device_current
I(Rb2):	0.000196872	device_current
I(Rb1):	0.000202085	device_current

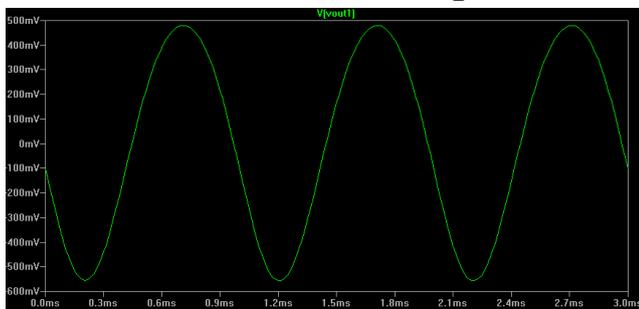


Fig. 11. DC and transient analysis of the first amplification stage driving a 1k Ω load, as depicted in Fig. 7

The DC analysis for the first stage matches closely with the calculated values in Section II, and it can be seen that the quiescent base current going through R_{B1} and R_{B2} is insignificant compared to the bias current. The output is a nearly distortionless swing that slightly exceeds 1V peak-to-peak.

B. The second common emitter stage

--- Operating Point ---

V(vb2):	1.16843	voltage
V(vc2):	6.96269	voltage
V(ve2):	0.455648	voltage
Ic(Q5):	0.287758	device_current
Ib(Q5):	0.00251653	device_current
Ie(Q5):	-0.290275	device_current
Ic(Q4):	0.00244151	device_current
Ib(Q4):	7.5022e-005	device_current
Ie(Q4):	-0.00251653	device_current
Ic(Q3):	0.00908373	device_current
Ib(Q3):	2.92352e-005	device_current
Ie(Q3):	-0.00911296	device_current
I(Rb4):	0.000973688	device_current
I(Rb3):	0.00100292	device_current

Fig. 12. DC analysis of the second amplification stage, depicted in Fig. 8

For the second stage, calculating the DC operating point yields a quiescent node emitter voltage is 0.45V, slightly below the desired value, while quiescent collector node voltage is nearly 7V for the common emitter amplifier. A perfect tradeoff that keeps $V_B > 0.5V$ and $V_C > 6.7V$ cannot seem to be achieved in simulation. At best, one of the bias resistors (R_{B3} in Fig. 8) is lowered to 10.4k Ω to bring V_C down to 6.56V and V_E up to 0.49V.

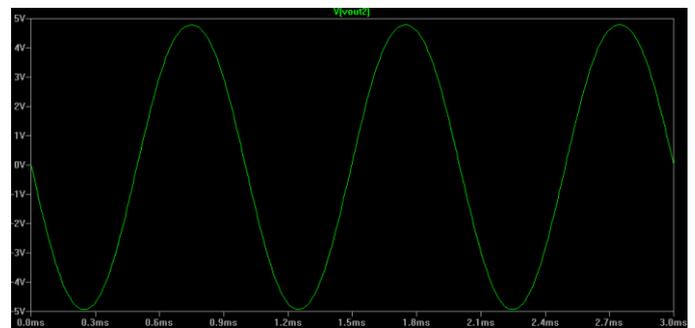


Fig. 13. Transient analysis of the second amplification stage driving a 500 Ω load, as depicted in Fig. 8, with $R_{B3} = 10.4k\Omega$

Despite having not enough room to swing, the generated output seems to be nearly free of clipping, though it falls slightly short of 10V peak-to-peak. Note that the quiescent collector current of the Darlington pair, indicated by $I_C(Q5)$ in Fig. 12, is 0.2A and requires the use of a transistor model with a better current rating than the 2N3904, such as the TIP41C transistor model. This is enough current to drive the next stage, which will further amplify the current for driving the load.

C. The push-pull output stage

The output stage is tested using a makeshift bias network defined by $R_{B,temp1}$ and $R_{B,temp2}$ that sets the quiescent base voltage of the pnp output transistor to 5V. The resistances of the network are deliberately chosen to be small to not affect the currents of the rest of the circuit.

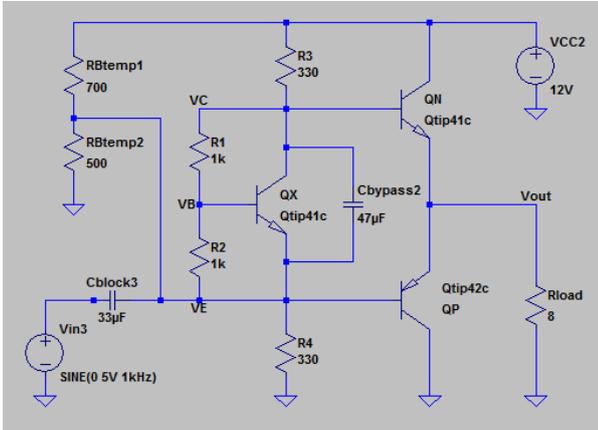


Fig. 14. Test circuit for the push-pull output stage, driving an 8Ω load representing a speaker

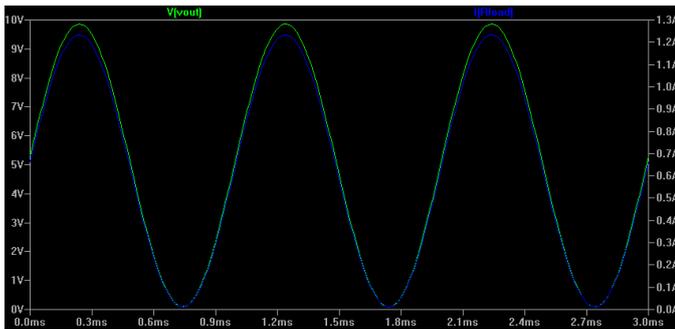


Fig. 15. Transient analysis for the push-pull output stage in Fig. 14, depicting both v_{out} and i_{load} on the same graph

Both the output voltage and current through the load is depicted in the figure above. The voltage swing is satisfactory and nearly distortionless, while the peak current matches the necessary amount needed to drive an 8Ω load with a peak voltage of 10V.

D. The complete audio amplifier

Putting all of the stages together as in Fig. 10 (again, with $R_{B3} = 10.4k\Omega$) provides the following results, which match closely with the results from previous simulation of only the output stage.

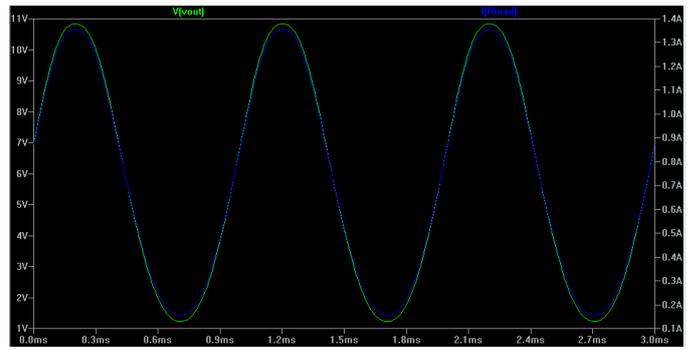


Fig. 16. Transient analysis for complete audio amplifier driving an 8Ω speaker load, as depicted in Fig. 10, with $R_{B3} = 10.4k\Omega$

The same analysis is repeated after adding emitter resistors at for the output transistors in order to account for thermal runaway. As expected, the gain decreases, resulting in an 8.5V peak-to-peak output swing.

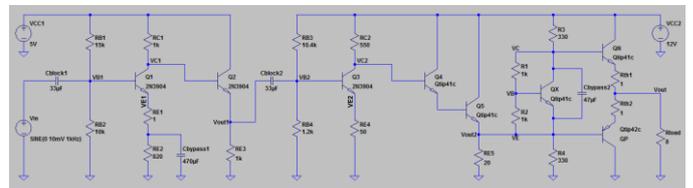


Fig. 17. Complete audio amplifier circuit accounting for thermal runaway

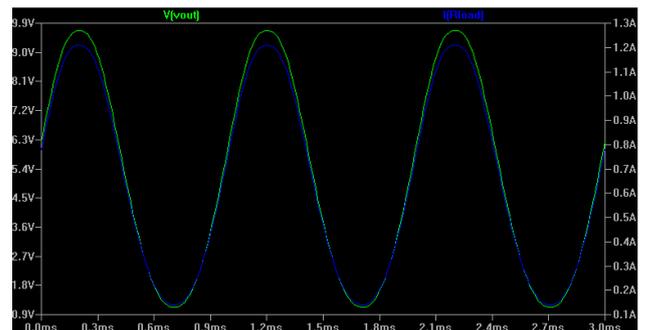


Fig. 18. Transient analysis for the audio amplifier accounting for thermal runaway in Fig. 17

Finally, the frequency response of the amplifier (without thermal runaway protection) is simulated as in the figure below and shown to satisfy the designated 3dB cutoffs.

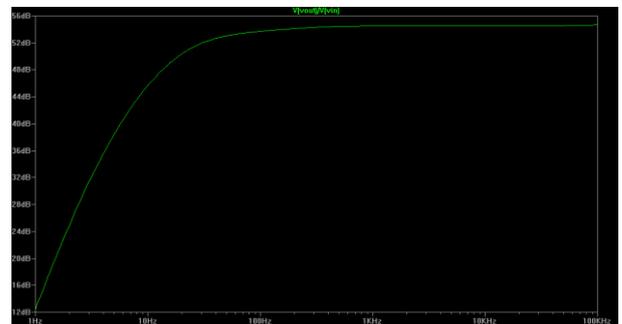


Fig. 19. AC analysis for the audio amplifier

IV. EMPIRICAL RESULTS

BEFORE the circuit is physically constructed, several resistors are changed due to the lack of availability of certain values in the laboratory. Referring to Fig. 10, $10.47\text{k}\Omega$ is used for R_{B3} ($10\text{k}\Omega$ in series with 470Ω), 552Ω is used for R_{C2} (470Ω in series with 82Ω), 51Ω is used for R_{E4} , and 20Ω is used for R_{E5} (two 10Ω power transistors in series). Simulating the amplifier with these values produces little variation in the output swing, as displayed in Fig. 19.

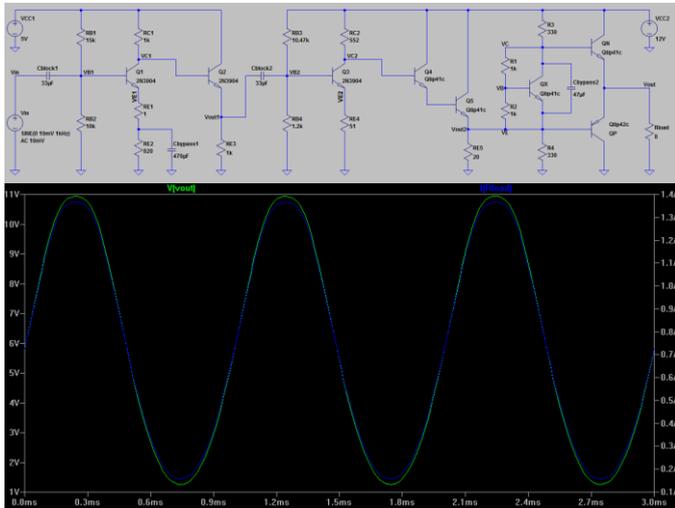


Fig. 20. Schematic and transient analysis for complete audio amplifier with actual resistor values

A. The first common emitter stage

The DC values for the first amplifier stage are found to be in close agreement with the theoretical and simulated values. Though the common emitter itself provides the expected 1V peak-to-peak output given a large enough load, directly biasing the emitter follower with the collector of the common emitter introduces extra noise at the input that is amplified at the output. The source of this noise is unknown, though it may be from the power supply. To work around this, the common emitter and emitter follower are decoupled using a DC blocking capacitor, and a separate bias network is used to establish the quiescent points for the follower (see Fig. 21). Using resistances of $100\text{k}\Omega$ for each of the bias network resistances maintains the gain for $1\text{k}\Omega$ load, verified through both simulation and experiment. The quiescent base current of the emitter follower is simulated to be $5.1\mu\text{A}$, while the bias current is $27.6\mu\text{A}$; though they do not differ by a factor of 10, circuit operation works just fine.

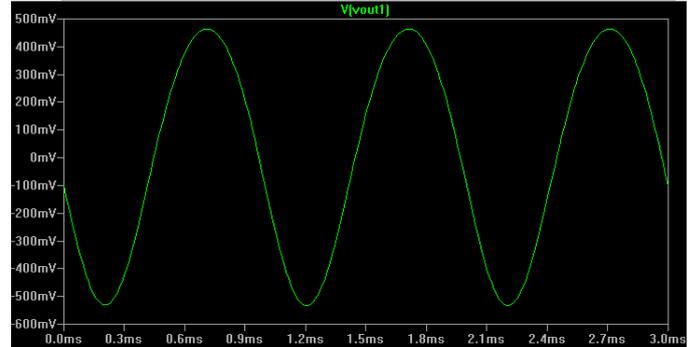
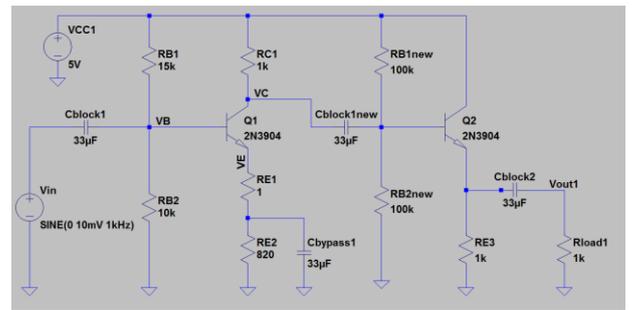


Fig. 21. Schematic and transient analysis for alternate design for first amplification stage

The operation of the actual circuit is tested by using a function generator to produce a 20mV peak-to-peak sine wave to be used as the input to the stage. The output closely matches the simulated swing of 1V peak-to-peak.

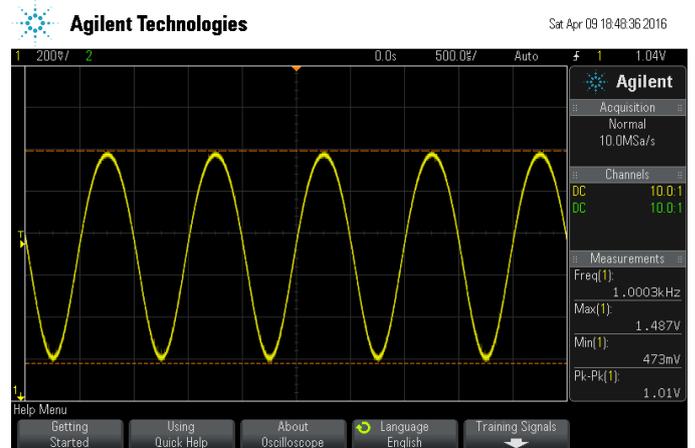


Fig. 22. Output waveform of first amplification stage as displayed on oscilloscope, where input is a 20mV peak-to-peak sine wave

B. The second common emitter stage

The DC values for the second amplifier stage are measured to be in close agreement with the theoretical and simulated values. However, the gain is less than expected: when a 1V peak-to-peak sine wave is used for the input, an 8.4V peak-to-peak output is produced (see Fig. 23). Furthermore, a grave issue arises when the first stage is linked to the second stage: a large quantity of high-frequency noise with an amplitude of a few hundred mV is introduced to the circuit. This appears to be due to the power supply; to mitigate these effects, a 0.01 μ F bypass capacitor is added between the 12V power supply and ground. This cuts down the noise considerably, but does not fully resolve the issue, which propagates to the output of the push-push stage and is the major source for distortion in this circuit. It should be noted that adding this capacitor may filter out desired frequencies in the audio signal, and hence there is a tradeoff between preserving the audio and denoising the circuit. At times, removing this capacitor can produce better sounding audio.

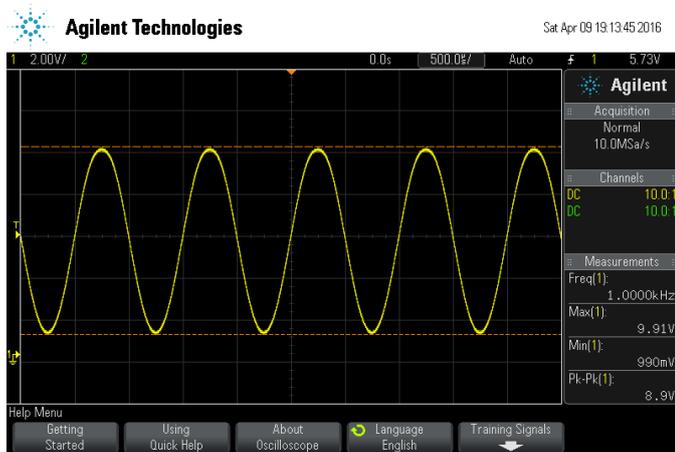


Fig. 23. Output waveform of second amplification stage as displayed on oscilloscope, where the input is a 1V input peak-to-peak sine wave

C. The push-pull output stage

Testing the push-pull stage driven by only the second stage with a 1V peak-to-peak input yields a lesser gain due to the shortcomings of the second stage, but still is able to drive an 8 Ω load effectively (see Fig. 24). The output swing is slightly less than that of the second stage at 8.8V, but this is to be expected because the push-pull stage has slightly below unity gain.

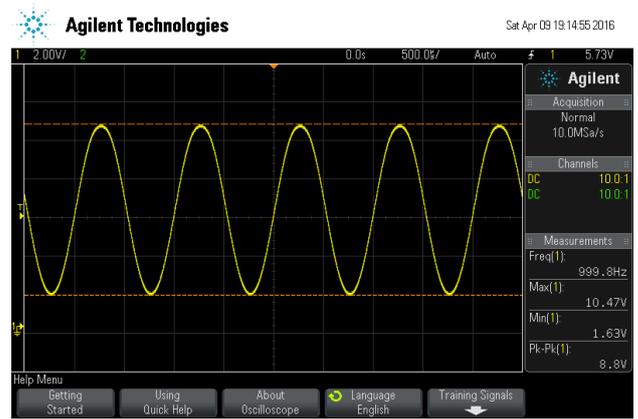


Fig. 24. Output waveform of push-pull stage driven by second stage as displayed on oscilloscope

D. The complete audio amplifier

Testing the aggregate audio amplifier yields an 8.4V peak-to-peak output from a 20mV peak-to-peak input. The maximum voltage the output can reach before clipping significantly is 9.2V peak-to-peak; this limitation on the output comes from the constraints of the second amplification stage. Note the distortion due to noise from the power supply, as mentioned earlier, manifested through an uneven thickness of the waveform.

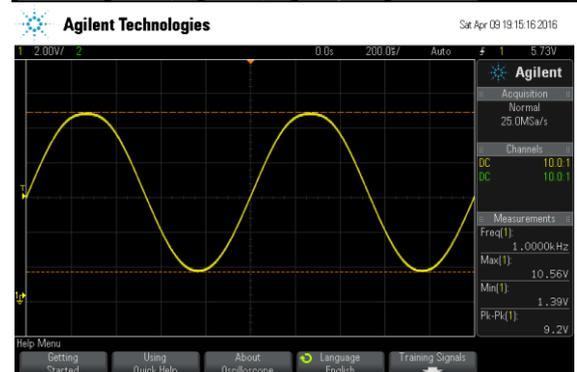
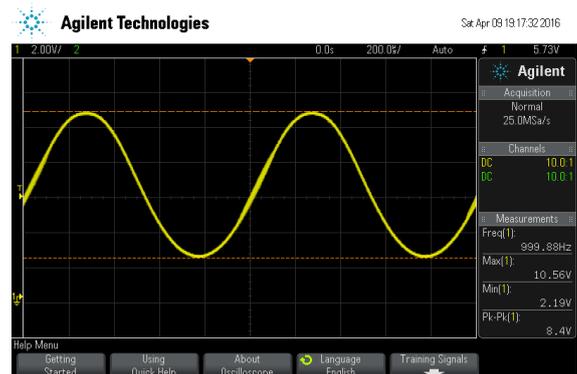


Fig. 25. Output waveforms of complete audio amplifier as displayed on oscilloscope. Top: output from 20mV input peak-to-peak sine wave. Bottom: Maximum output swing possible before clipping

E. 3dB Points

To determine whether the desired higher and lower 3dB frequencies are satisfied, a frequency sweep is conducted with a 20mV peak-to-peak input sine wave. The output waveform is observed at various frequencies ranging from 100Hz to 100kHz. The 3dB points are shown to be satisfied, with slight distortions at both extremes, though the overall gain seems to have decreased for the circuit as opposed to earlier results (perhaps due to significant temperature increases). Improvements to the lower 3dB cutoff can be made by changing $C_{bypass2}$ to a higher value, such as 470 μ F, though this has only been successfully tested in simulation.

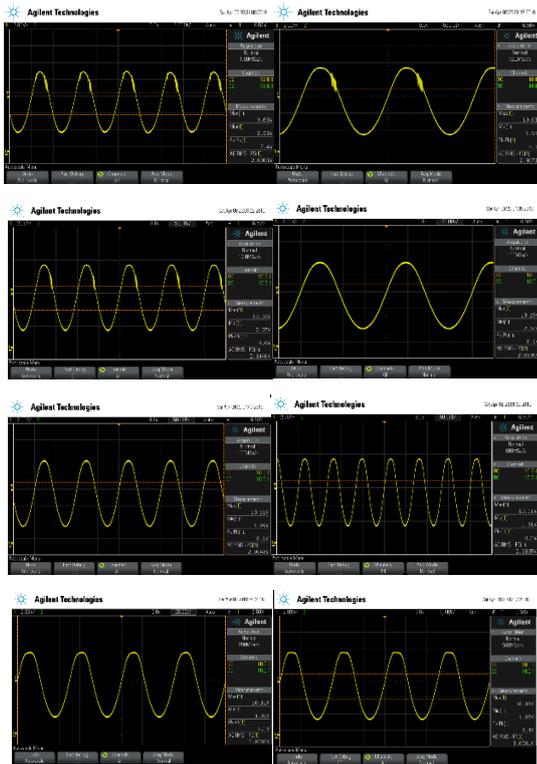


Fig. 26. Output waveforms of audio amplifier with inputs of various frequencies. Order of frequencies: 100Hz, 500Hz, 1kHz, 5kHz, 10kHz, 20kHz, 40kHz, 100kHz

F. Data Tables

Quiescent Points

Node	Theoretical	Simulation	Empirical
Emitter (stage 1)	1.3V	1.3V	1.34V
Base (stage 1)	2V	1.97V	1.96V
Collector (stage 1)	3.4V	3.41V	3.43V
Emitter (stage 2)	0.5V	0.46V	0.5V
Base (stage 2)	1.2V	1.21V	1.24V
Collector (stage 2)	6.7V	6.56V	6.62V

Output Swings with 20mV Peak-to-Peak Input at 1kHz

Node	Theoretical	Simulation	Empirical
Stage 1	0.98V-1V	1.07V	1.01V
Stage 2	9.7V-9.9V	9.71V	8.8V
Stage 3	<9.7-9.9V	9.67V	8.4V

Frequency Sweep Results (Empirical Only)

Frequency	Output Swing	RMS
100Hz	7.4V	2.63V
500Hz	8.1V	2.91V
1kHz	8V	2.84V
5kHz	8.1V	2.88V
10kHz	8.1V	2.9V
20kHz	8.2V	2.94V
40kHz	8.2V	2.96V
100kHz	8.4V	3.05V

Summarizing these results, the main issue seems to arise from the second stage of the audio amplifier, which provides a lower gain than intended. Otherwise, the behavior of the amplifier is consistent with the device's specifications. It should be noted that early test trials have produced a 9.2V swing from a 20mV input swing, but the circuit performance seems to have degraded over time. Further research will go into improving the second common emitter stage and maintaining its consistency.

V. CONCLUSION

It is virtually physically impossible to construct an audio amplifier from basic discrete components without any distortion. With the introduction of operational amplifiers and capitalizing on negative feedback, these issues can be resolved much easier. With only the tools available for this lab, there are many tradeoffs to keep in mind, especially having to do with gain and the available headroom. The circuit must be designed to optimize both, which are highly dependent on one another. With that being said, it is eye-opening to observe how such cheap components can be used to construct a functional amplifier, albeit with some defects.